Exhibit 7

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

MONTEREY RESEARCH, LLC, Plaintiff, v. RENESAS ELECTRONICS CORPORATION, et al., Defendants.	Case No. 2:24-cv-00238-JRG JURY TRIAL DEMANDED

DECLARATION OF TAKAHIRO GOTO

1. My name is Takahiro Goto. I am an engineer employed by DENSO Corporation in its Semiconductor-Originated Key Technologies R&D Division. I have been employed by DENSO Corporation since January 2002, and my current job title is General Manager.

2. I am generally familiar with the microcontrollers and microprocessors (collectively, "semiconductor chips") used in products manufactured by DENSO Corporation and its affiliate DENSO International America, Inc. (collectively referred to herein as "DENSO"). I am also generally familiar with the semiconductor technologies used in those semiconductor chips.

3. I have reviewed the Complaint filed by Monterey Research LLC ("Monterey") against DENSO and one of its semiconductor chip suppliers, Renesas Electronics Corporation ("Renesas"). The Complaint makes clear that the patent infringement allegations contained therein are directed to the circuit design and physical structure of the semiconductor chips manufactured by Renesas. For example,

- Monterey's '300 patent allegedly relates to methods for erasing memory cells in solid state memory devices by combining neutralizing holes with spillover electrons within a memory cell, see Complaint ¶ 28;

- Monterey's '968 patent allegedly relates to memory device with a negative voltage generating circuit that applies a negative voltage to a word line of a memory cell array and a positive voltage generating circuit that applies a positive voltage to a well of the memory cell array when the negative voltage reaches a predetermined voltage during an erase operation of the memory cell array, and methods for erasing the memory cell array, id. ¶ 41;
- Monterey's '133 patent allegedly relates to a circuit for performing a reset function at certain voltage levels to avoid data corruption or other faulty operations, id. ¶¶ 51, 53; and
- Monterey's '688 patent allegedly relates to a circuit with digital and analog circuit blocks on the same chip, id. ¶ 65.

For ease of reference, I will refer to the circuit design and physical structure that the Complaint states are relevant to Monterey's infringement allegations as the "accused features" of Renesas semiconductor chips.

4. To the extent Renesas semiconductor chips include the accused features, those accused features are fixed during the manufacture of the semiconductor chips before DENSO purchases or receives the semiconductor chips and at a level not accessible to DENSO. DENSO lacks knowledge and information of the specific and detailed circuit designs for the accused features in the Renesas semiconductor chips it purchases.

5. DENSO cannot and does not modify the Renesas semiconductor chips it purchases in any way with respect to the accused features. As indicated above, those features relate to the circuit design and physical structure of semiconductor chips that are entirely outside DENSO's control.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on: September 13th, 2024 Takahiro Goto